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MS-7697 Ver:1.0

CPU:

AMD FM1

System Chipset:

AMD - Hudson D3

On Board Chipset:

USB2.0 RearX4 FrontX4

USB3.0 RearX2 FrontX2

SATAIII X6

LPC Super I/O --F71869A

LAN-Realtek 8111E

Azalia CODEC - Realtek ALC887 Co-lay 892

Main Memory:

DDR III *2 (Max 16G)

Expansion Slots:

PCI Express X16 Slot * 1

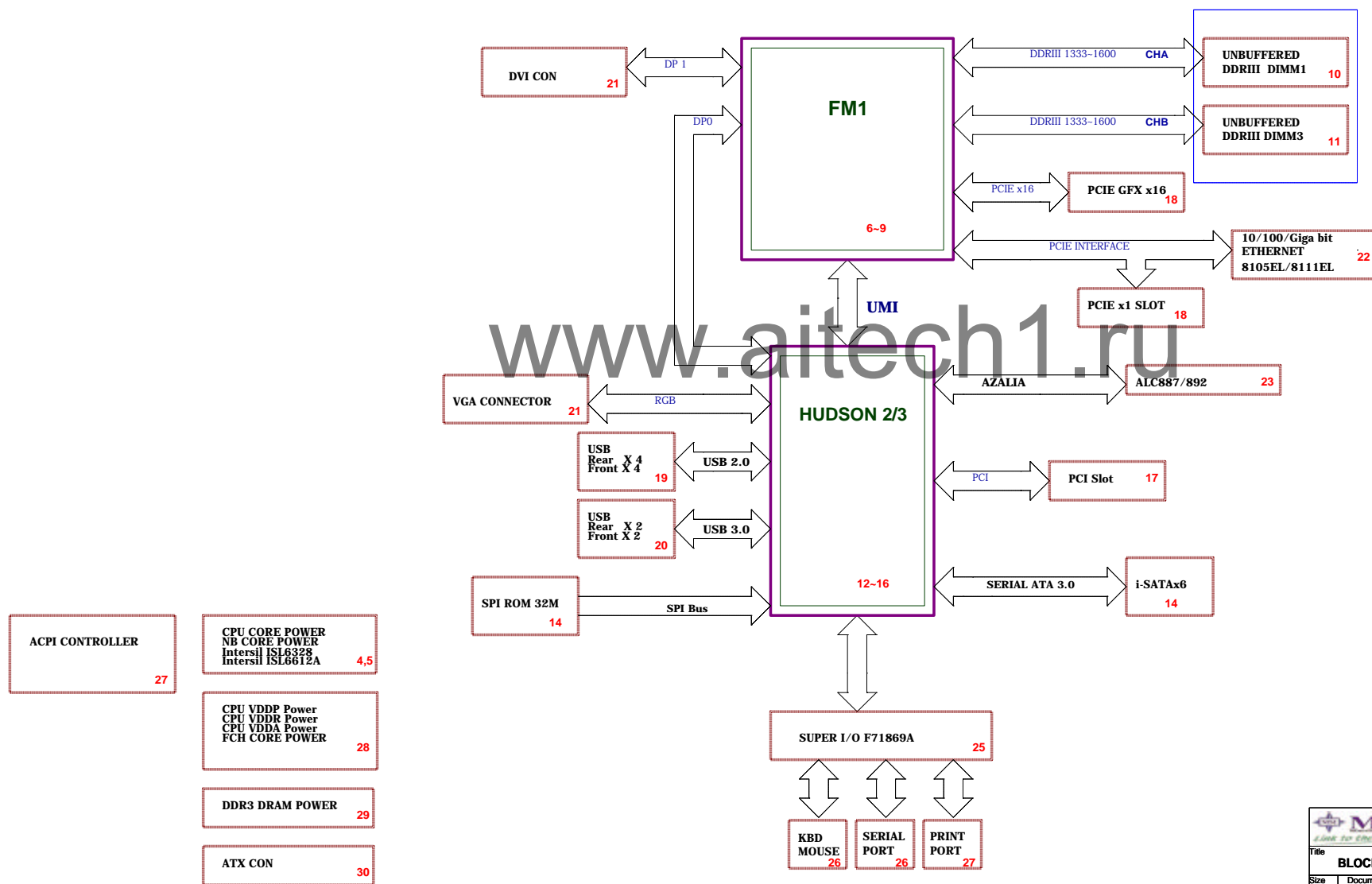
PCI Express X1 Slot * 2

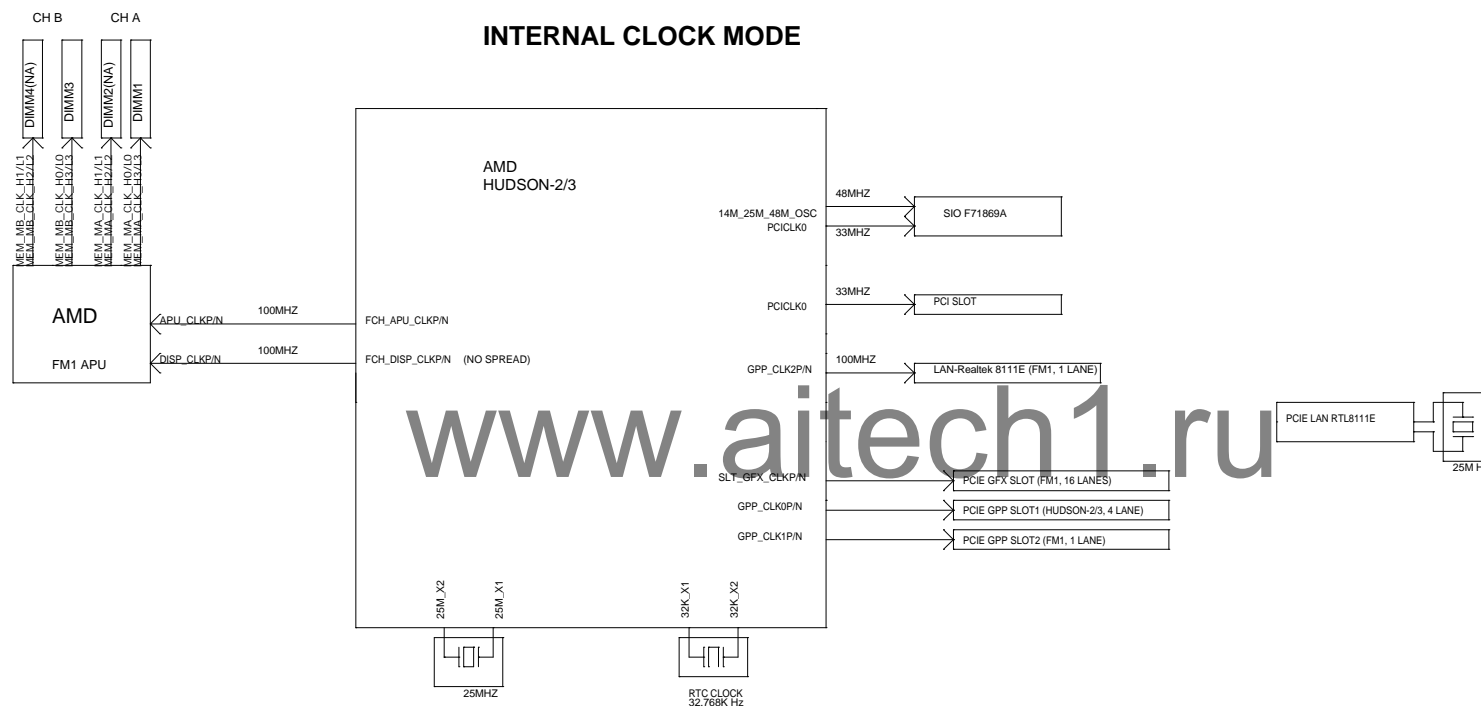
PCI Slot * 1

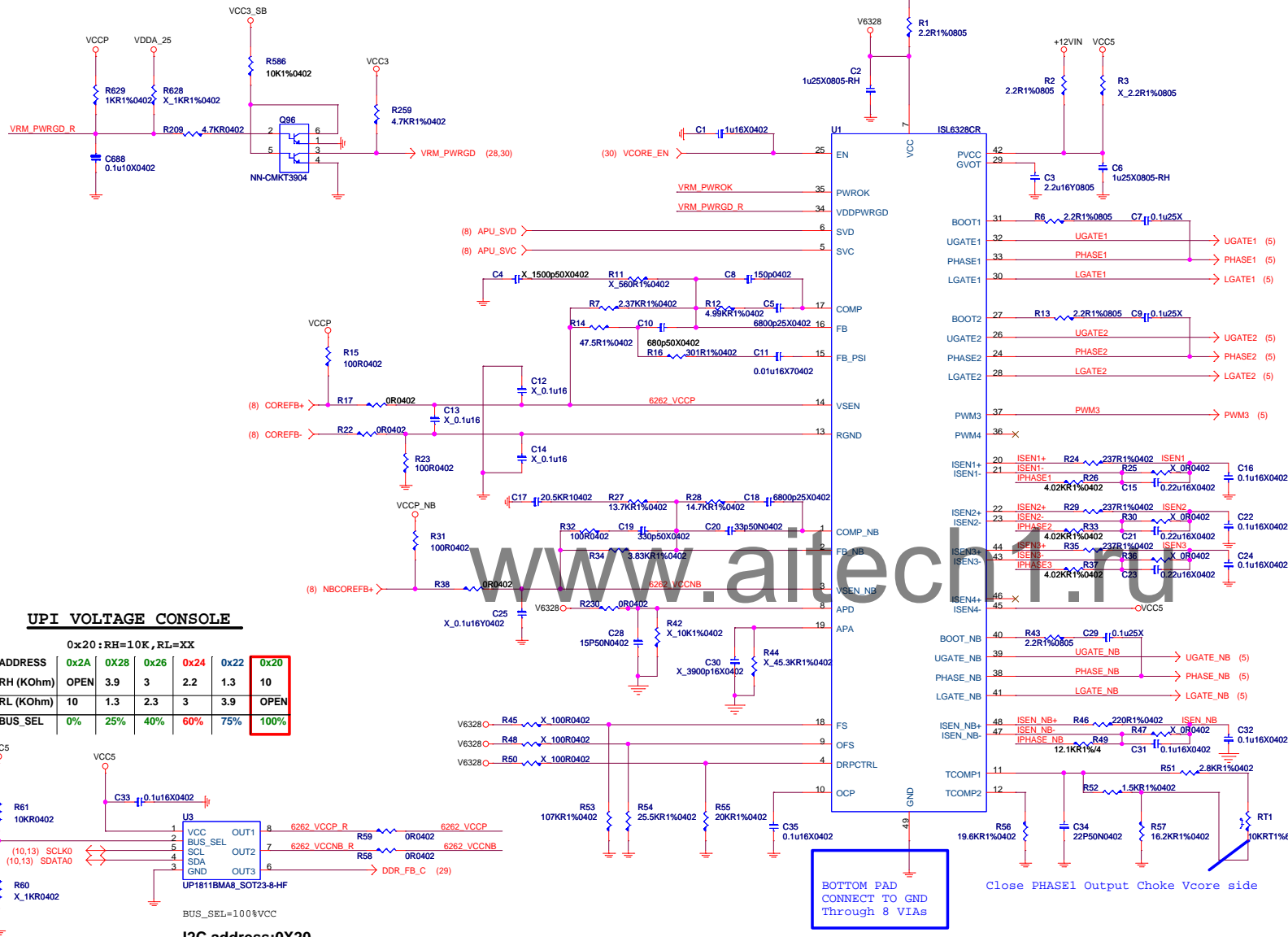
VRM

Controller - Intersil ISL6328 3+1 Phase

FUSION BLOCK DIAGRAM



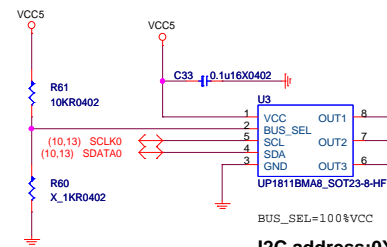




UPI VOLTAGE CONSOLE

0x20 : RH=10K, RL=XX

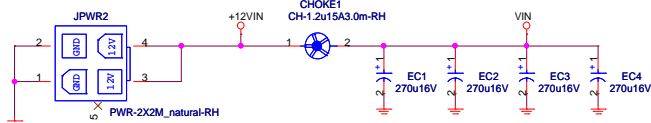
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

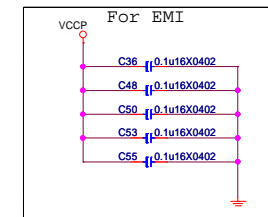
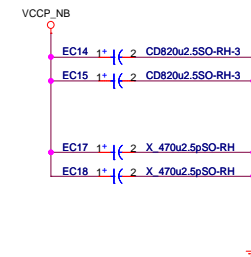
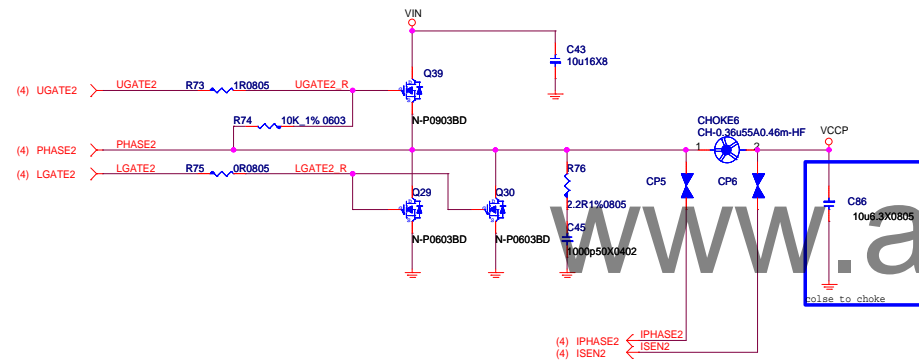
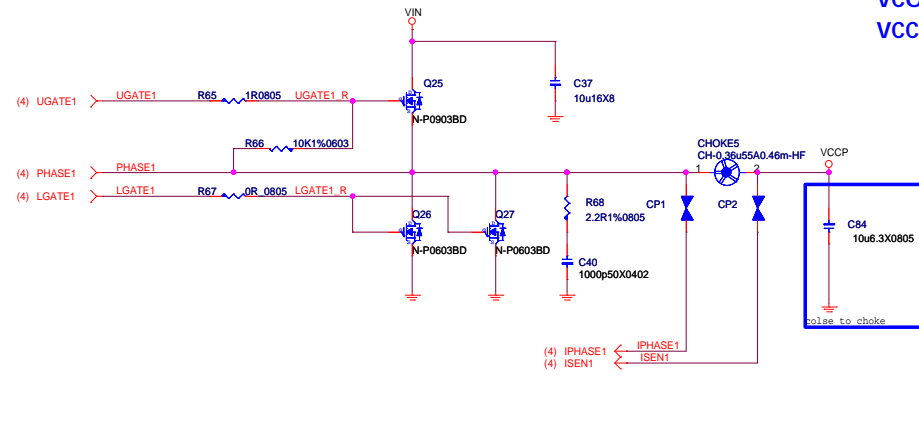


I2C address:0X20

BOTTOM PAD
CONNECT TO GND
Through 8 VIAs

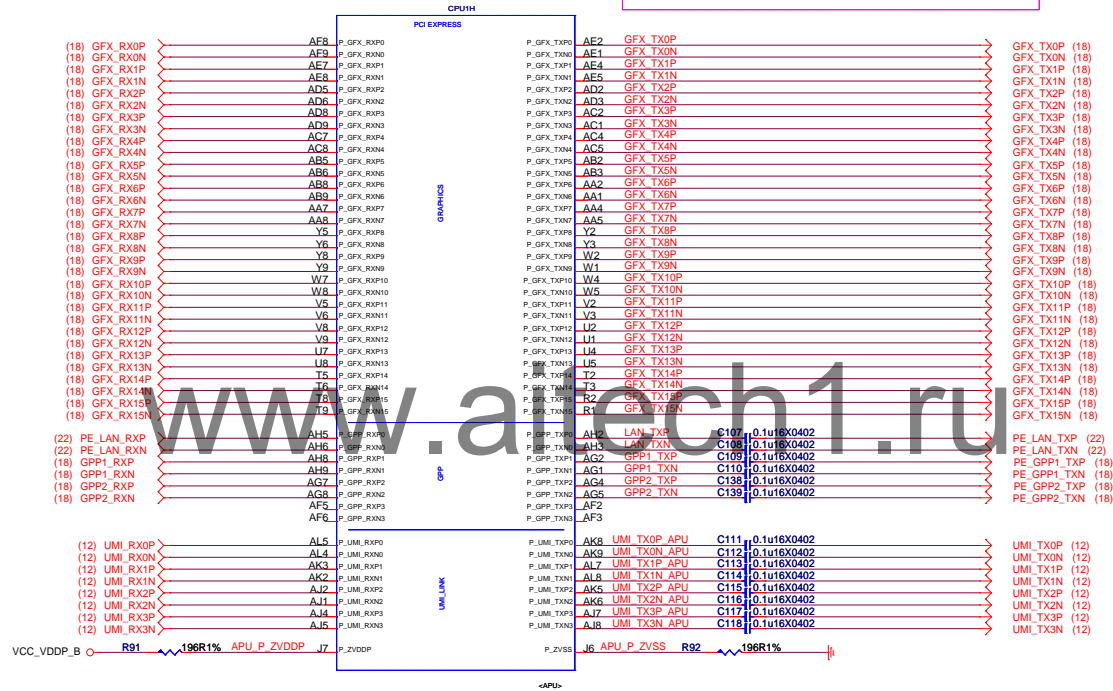
Close PHASE1 Output Choke Vcore side



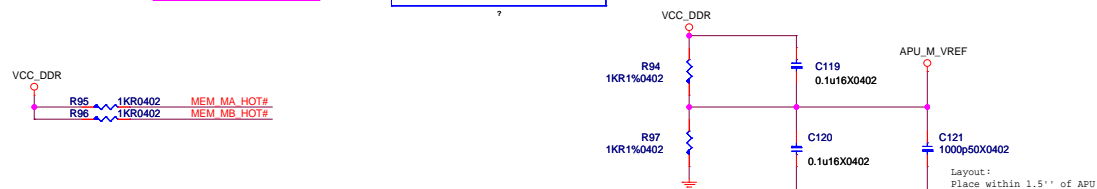
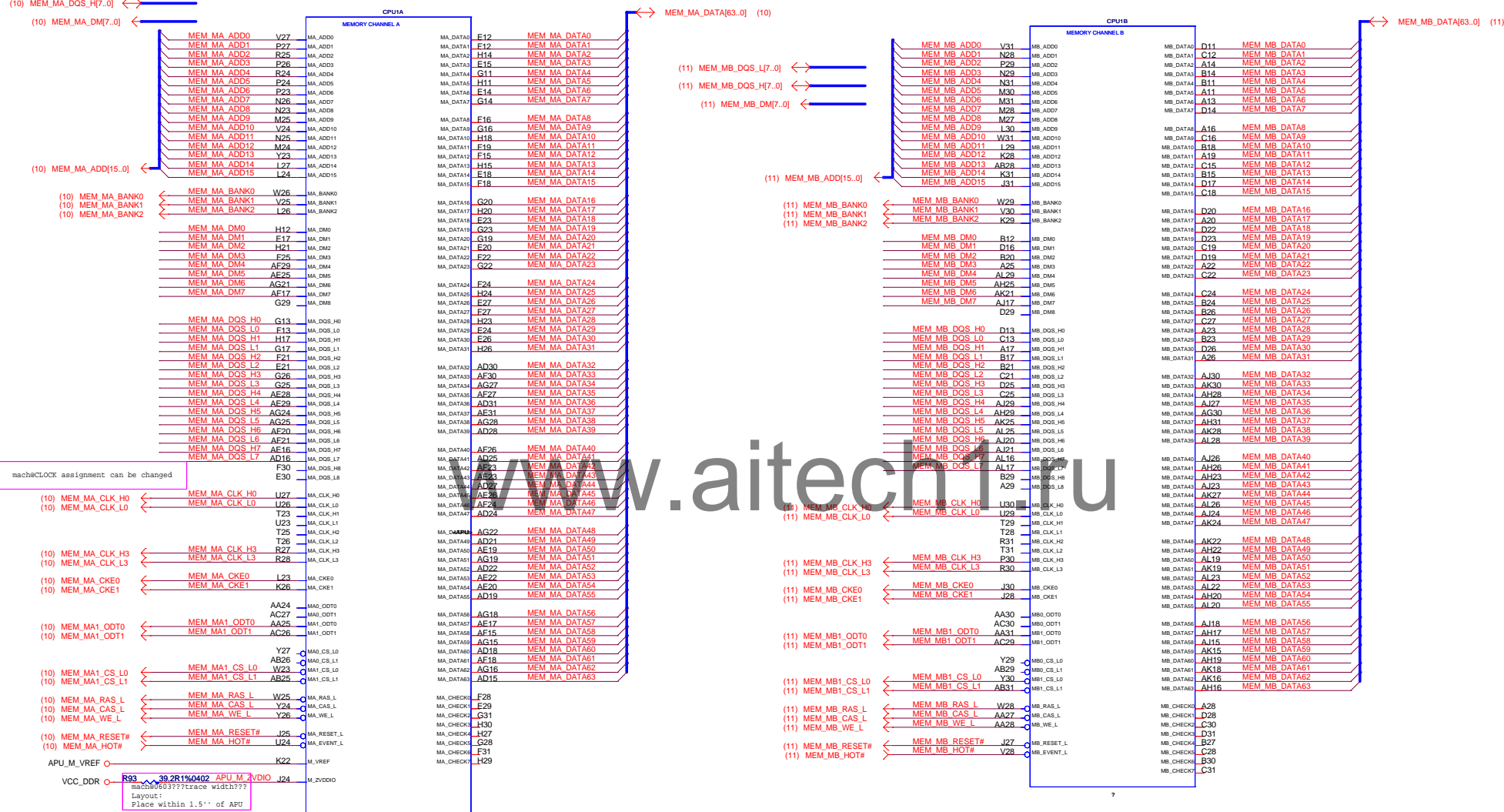


FM1 PCIE I/F

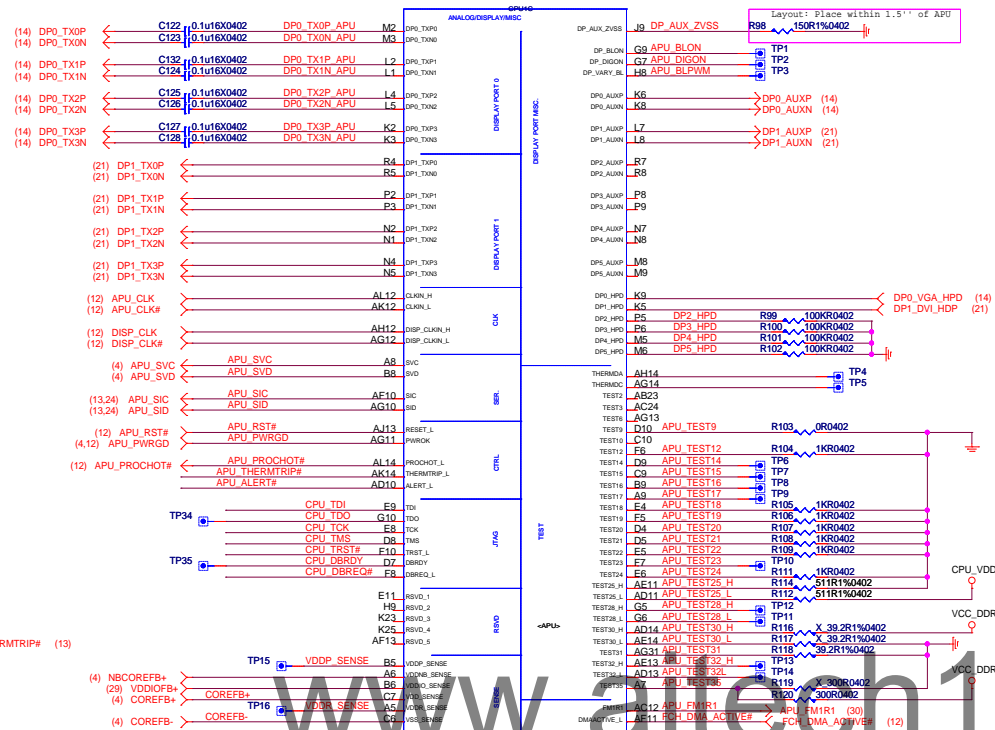
mach@CRB PCIE AC Capacitors:75nF to 200nF
Layout: PLACE CAPS WITH APU < 1 INCH
ROUTE ALL PCIE AS 85OHM +/-10%



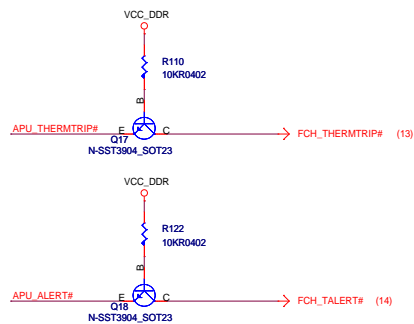
(10) MEM_MA_DM[7..0] ←



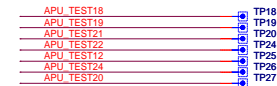
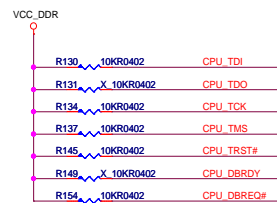
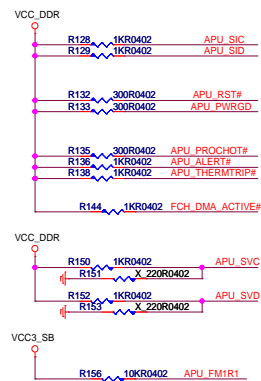
FM1 DISPLAY I/F

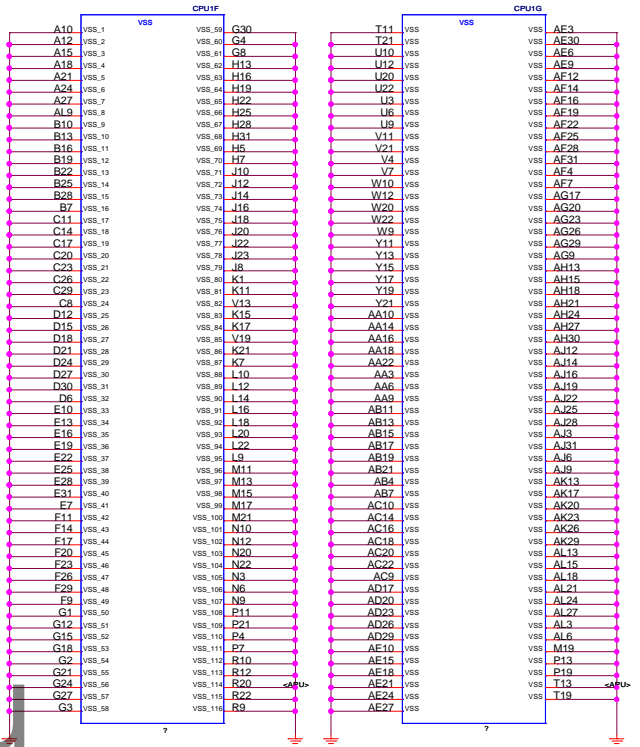
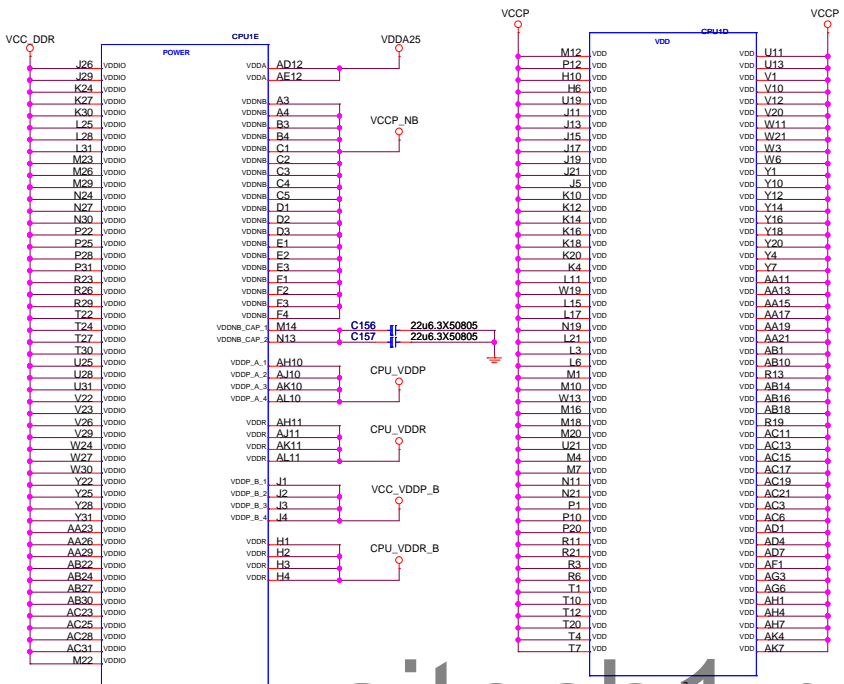
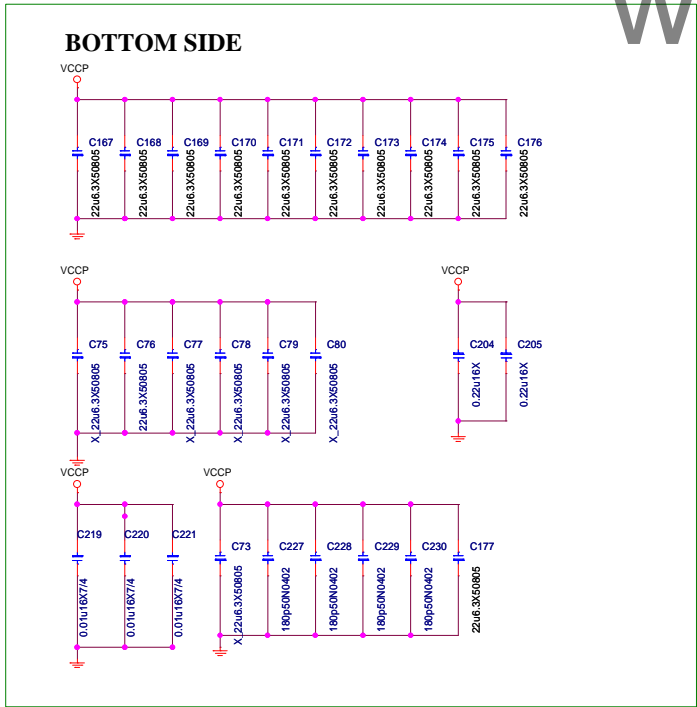
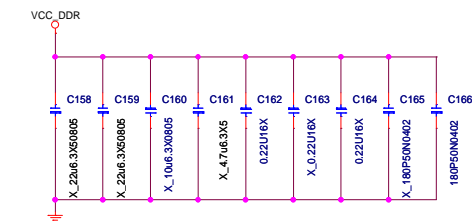
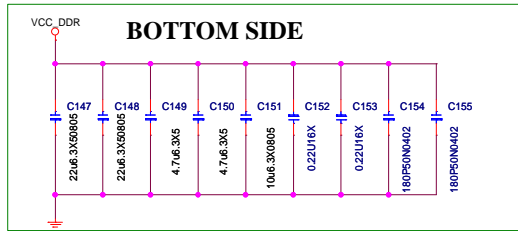
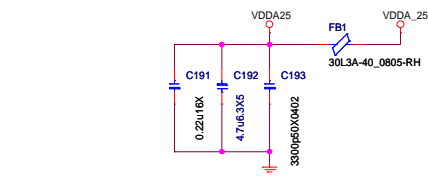


SCAN Connector



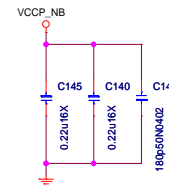
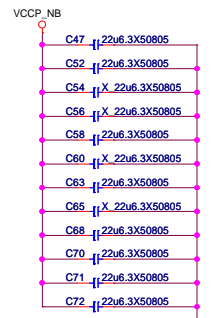
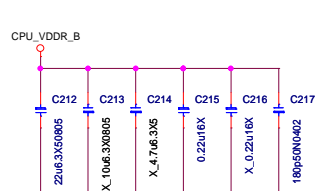
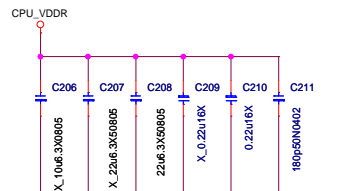
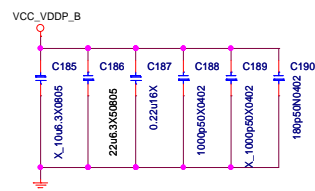
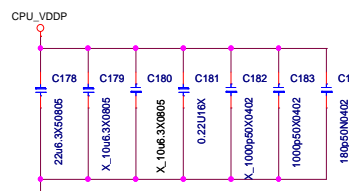
PULL UP

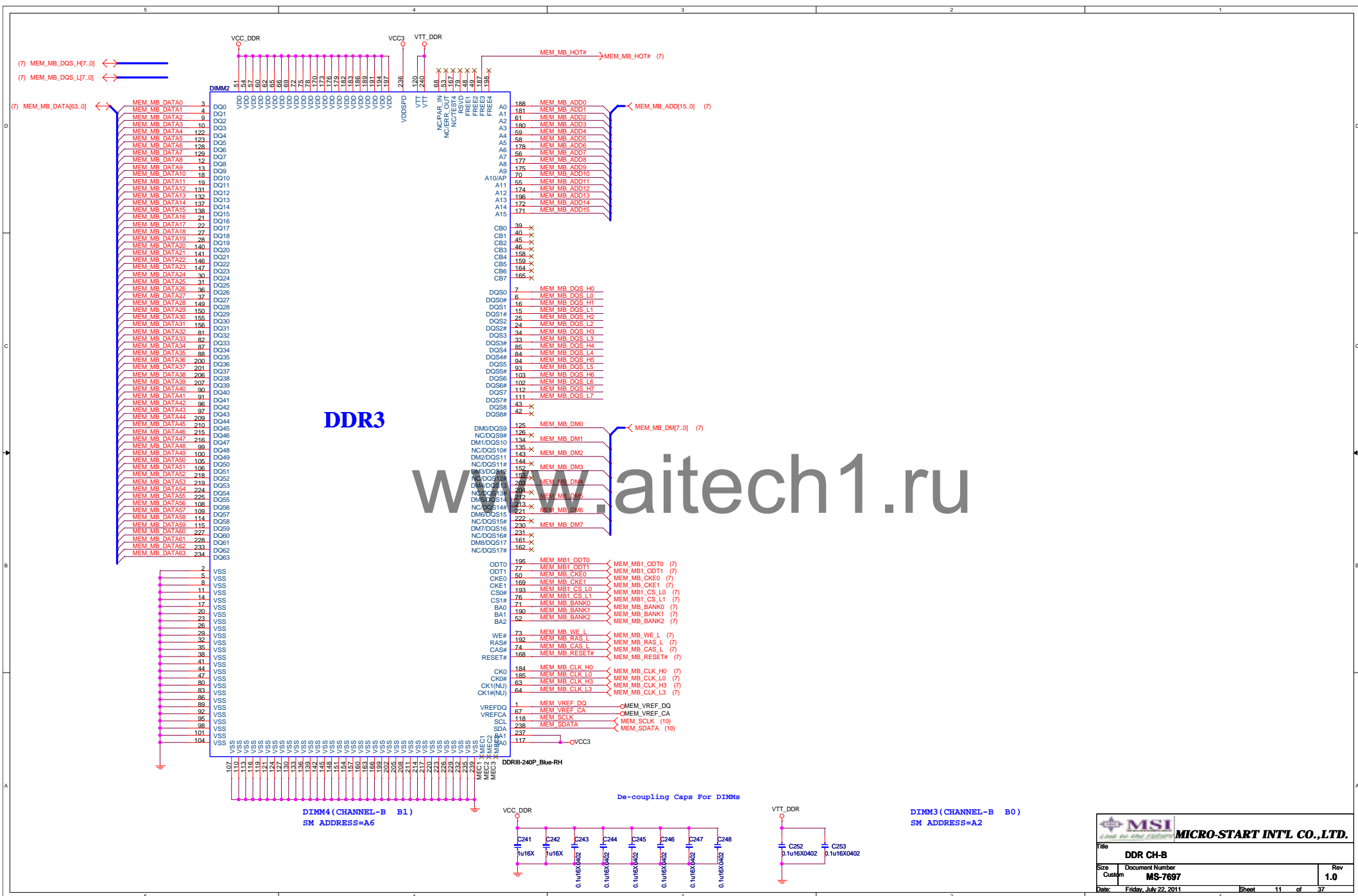




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VDDP and VDDR support two separate power planes with single regulator

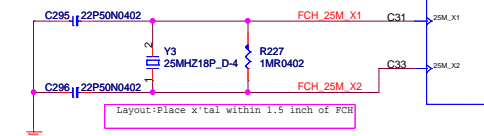
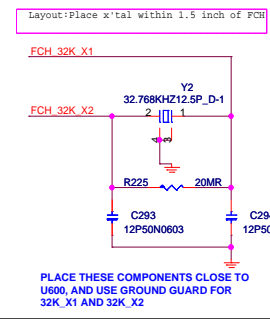
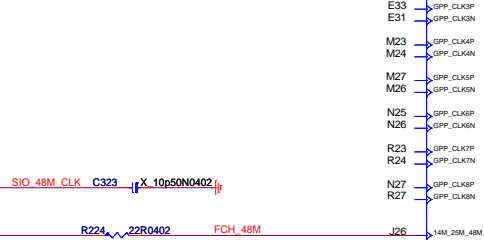
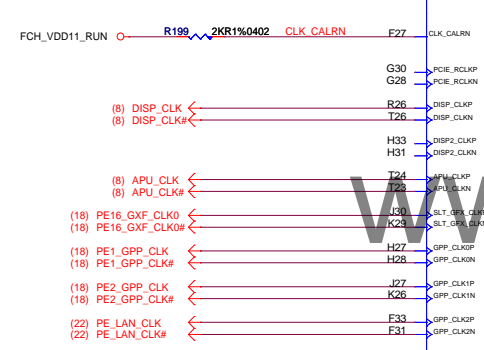
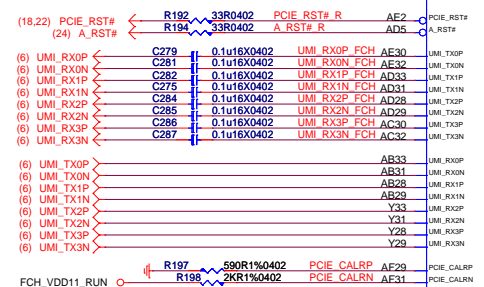




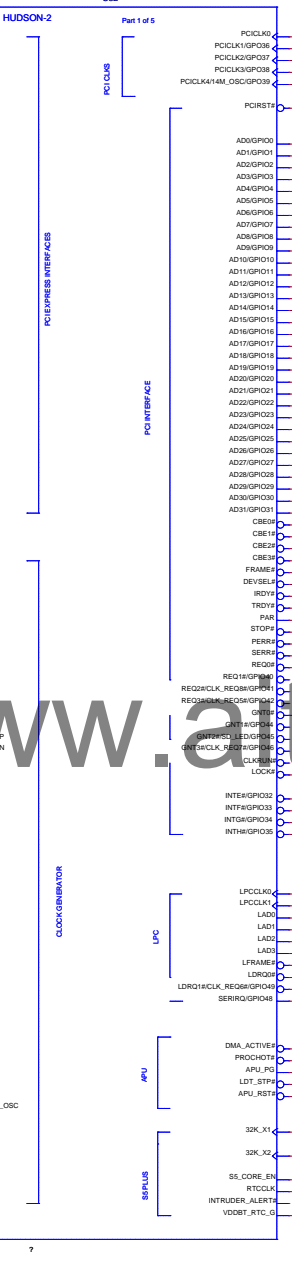
To PCIEX16, X1, LAN
To SIO

PCIE_RST#
A_RST#

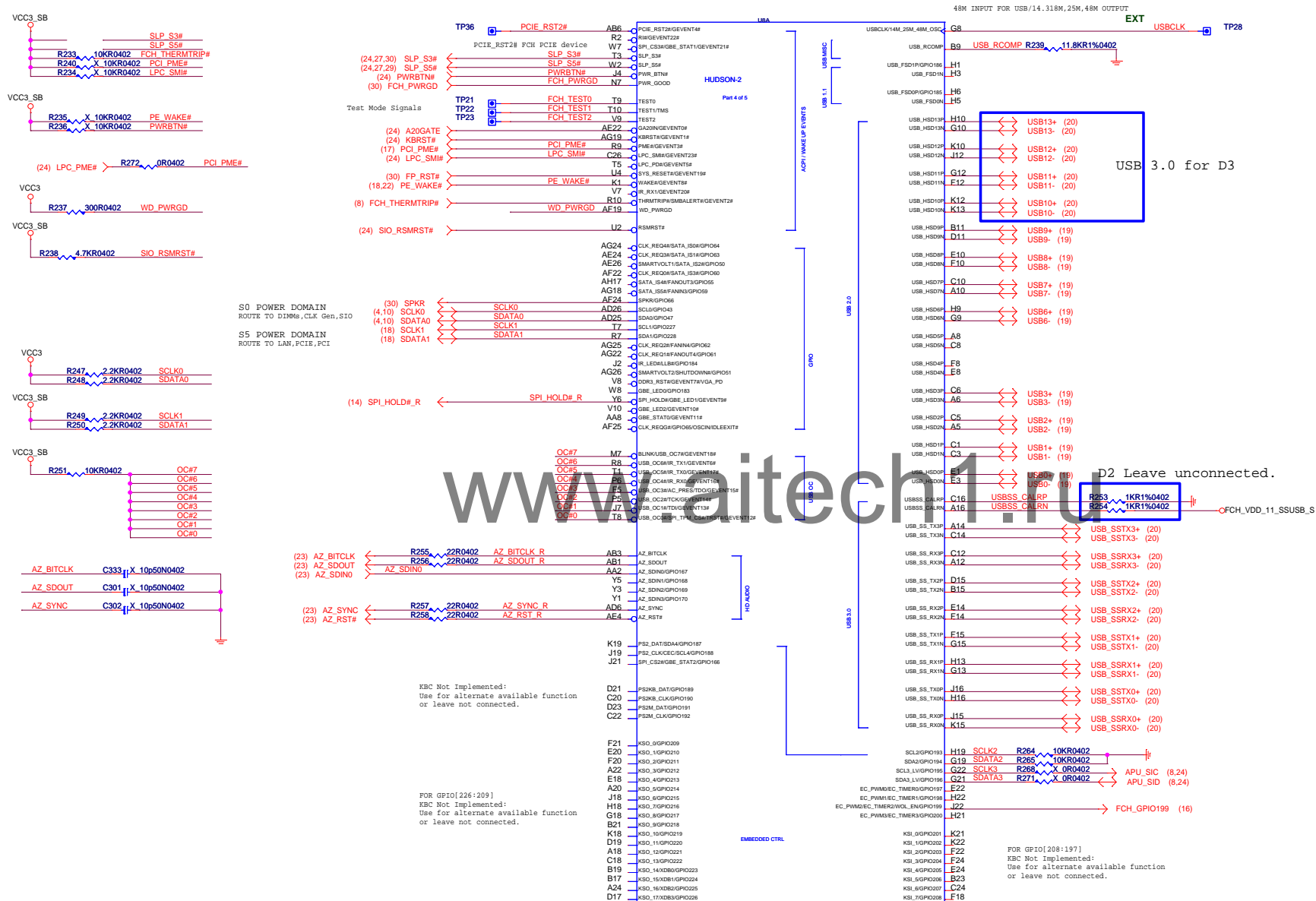
A_RST# for LPC device:
PCIE_RST# for APU PCIE device:
PCIE_RST# FCH PCIE device

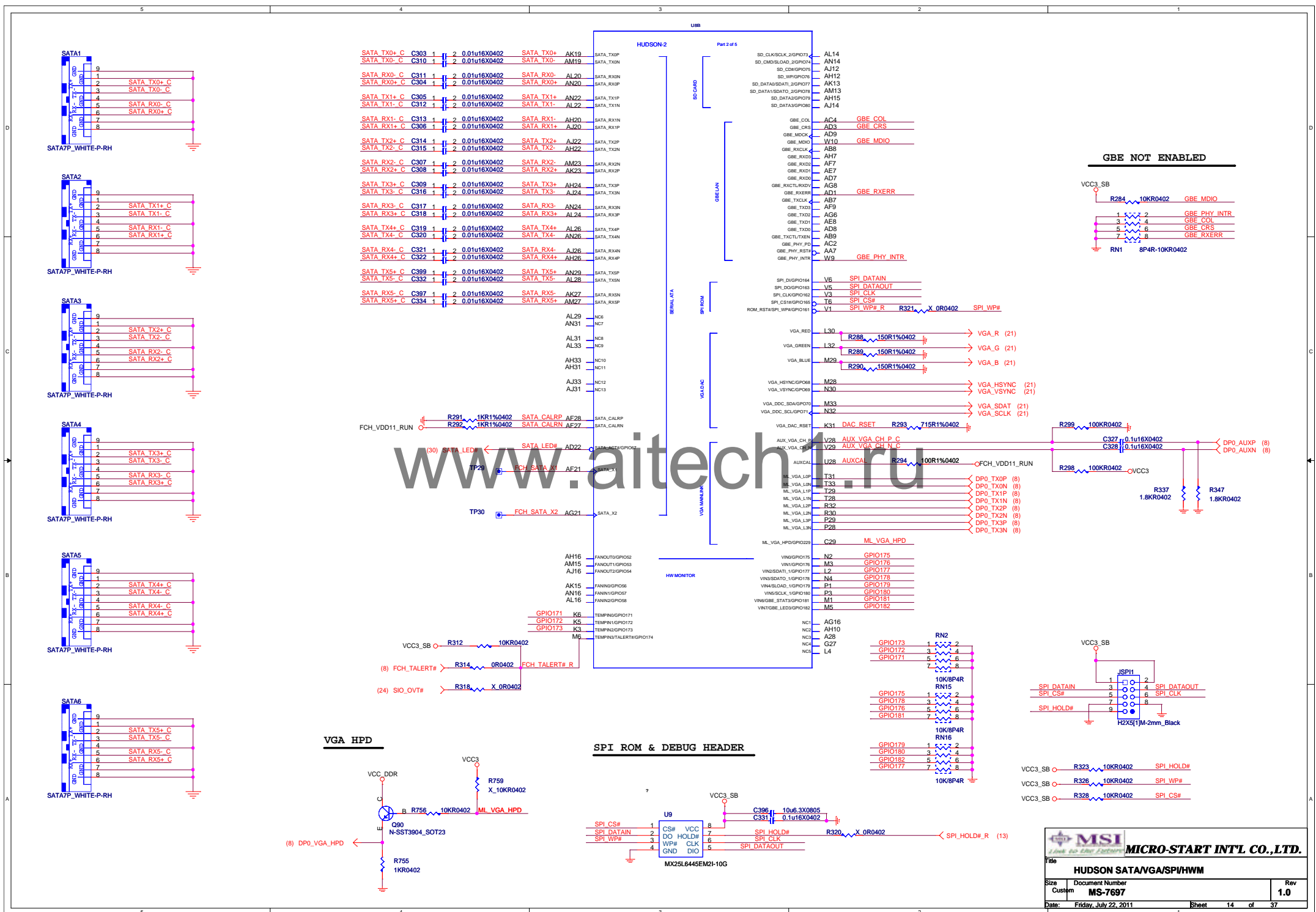


Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the APU I/O rail. They are also in the S5 domain to prevent glitching at power up.

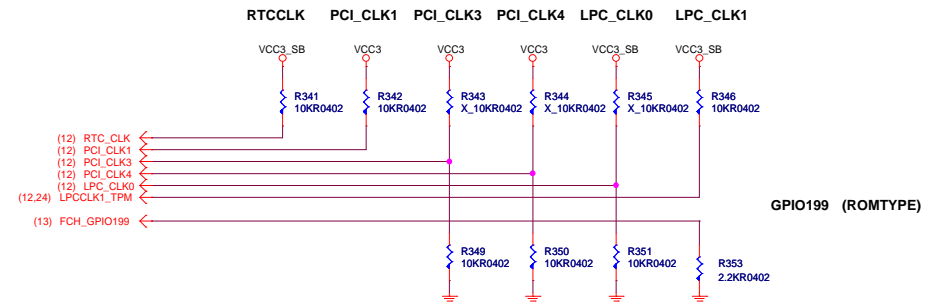


HUDSON ACPI/USB/AZ/GPIO





FCH REQUIRED STRAPS



	RTCCCLK	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO199 (ROMTYPE)
PULL HIGH	S5 Plus MODE DISABLED DEFAULT	PCIe interface at Gen2 DEFAULT	Enable Debug Straps	Reserved	EC ENABLED	Internal clock mode DEFAULT	LPC ROM
PULL LOW	S5 Plus MODE ENABLED	FORCE PCIe at Gen1	Disable Debug Straps DEFAULT	APU_CLK/DISP_CLK Required setting DEFAULT	EC DISABLED DEFAULT	External clock mode	SPI ROM DEFAULT

*This strap is not
used in External
clock mode

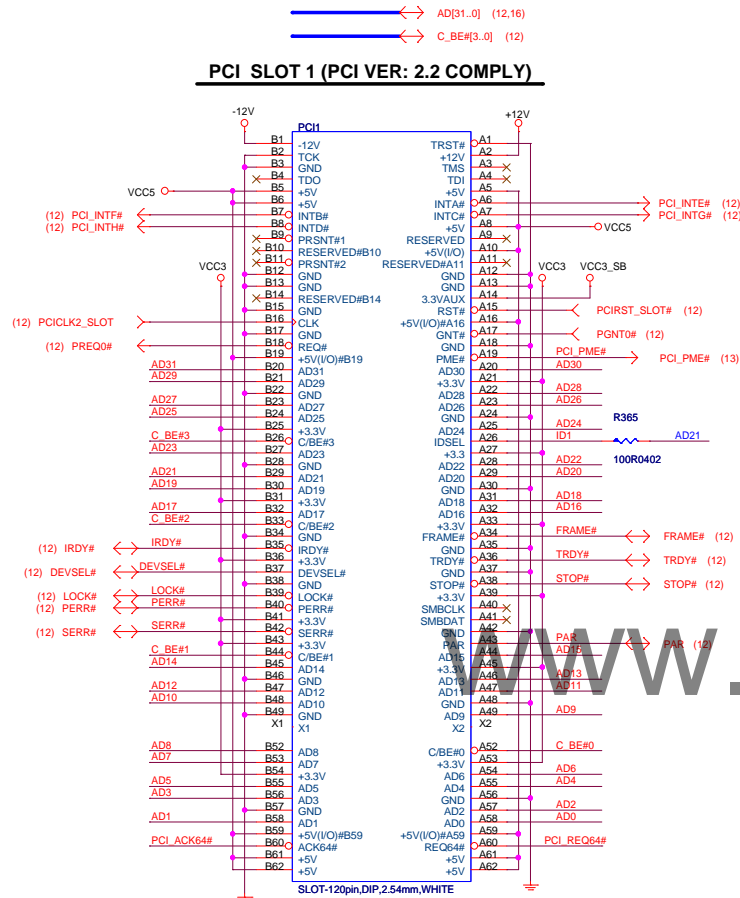
FCH DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	Use internal PLL clock DEFAULT			Disable I2C ROM DEFAULT	Use ROMTYPE straps DEFAULT
PULL DOWN	Bypass Internal PLL clock			Enable loading settings for UMI/PLL/misc from I2C ROM	Boot from PCI bus

Layout:
VSSPL_SYS/VSSAN_HWM CONNECT TO GND
WITH A SEPRATED VIA

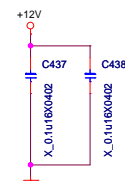
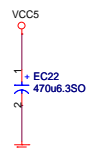
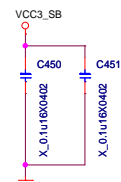
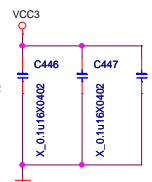
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



IDSEL = AD21

MASTER = PCI_REQ#0

PCI_GNT#0



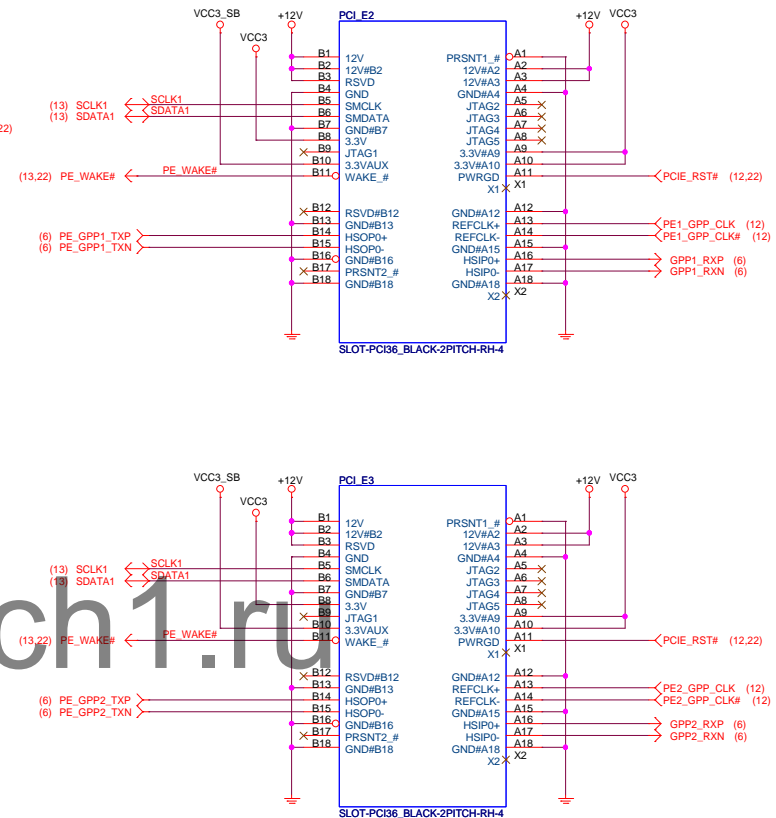
PCI EXPRESS x16 Slot



PCI Express X16 slot(X1)

+12V	- 5.5 A
+3.3Vaux (wake)	- 375mA
+3.3Vaux (no wake)	- 20mA
+3.3V	- 3.0A

PCI EXPRESS X1 Slot-1



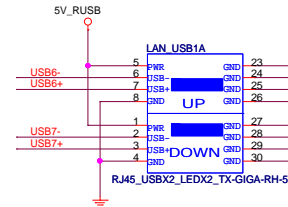
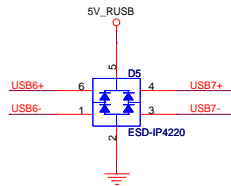
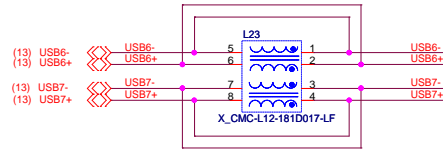
PCI Express X1 slot (X2)

+12V	- 1 A
+3.3Vaux (wake)	- 750mA
+3.3Vaux (no wake)	- 40mA
+3.3V	- 6.0A

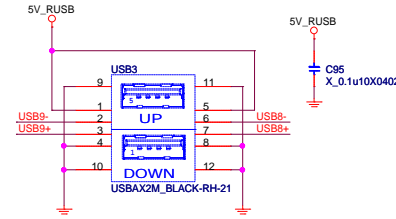
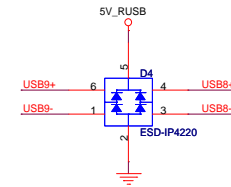
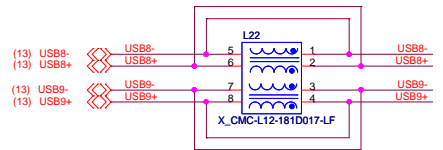
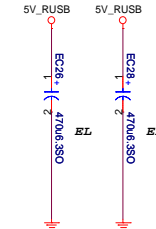


File	PCI EXPRESS X16
Size	Custom
Document Number	MS-7697
Date	Friday, July 22, 2011
Sheet	18 of 37
Rev	1.0

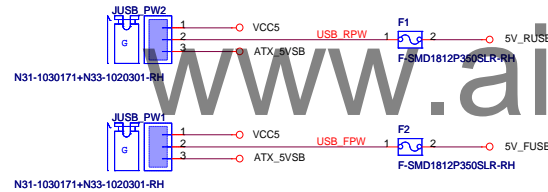
POWER CIRCUIT FOR USB PORT 0,1



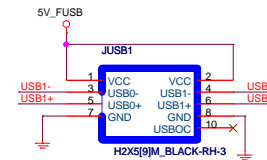
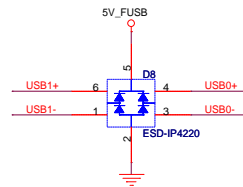
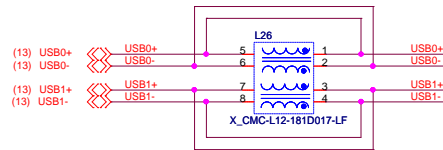
NEAR USB REAR CONNECTOR



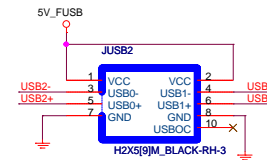
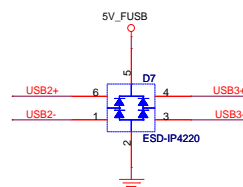
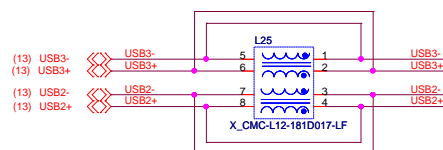
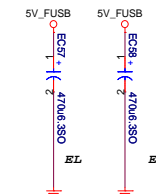
Near Rear ==>

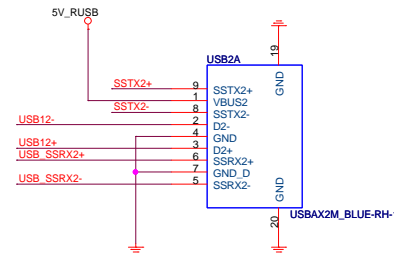
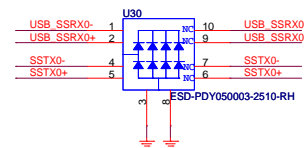
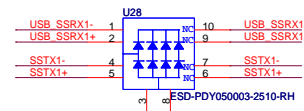
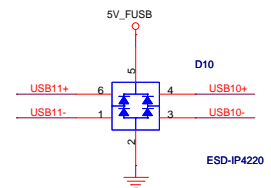
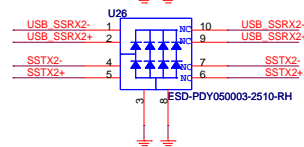
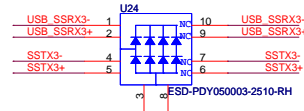
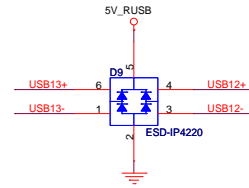
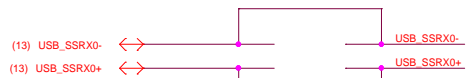
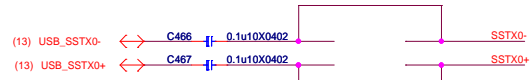
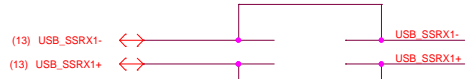
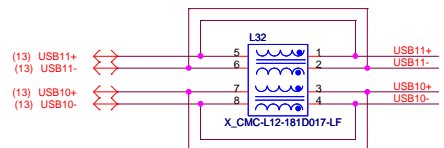
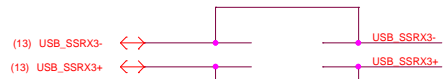
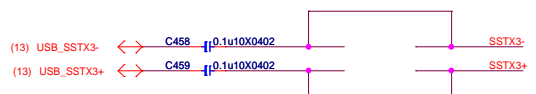
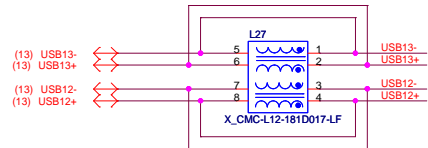
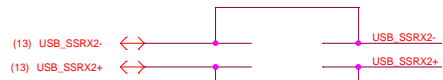


Near Front ==>

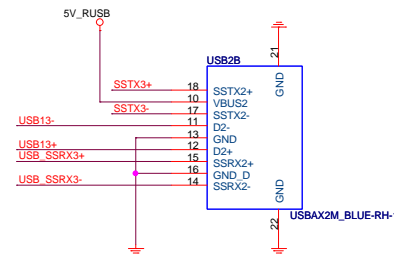
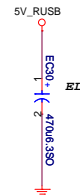


NEAR USB Front CONNECTOR

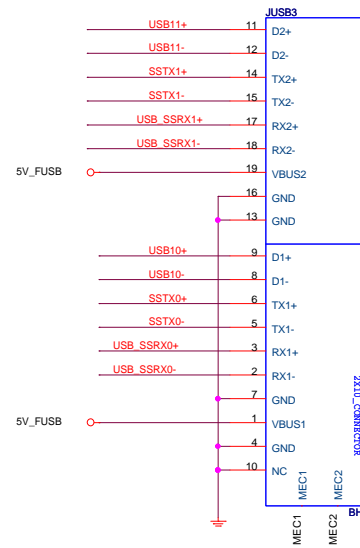
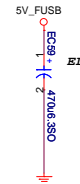




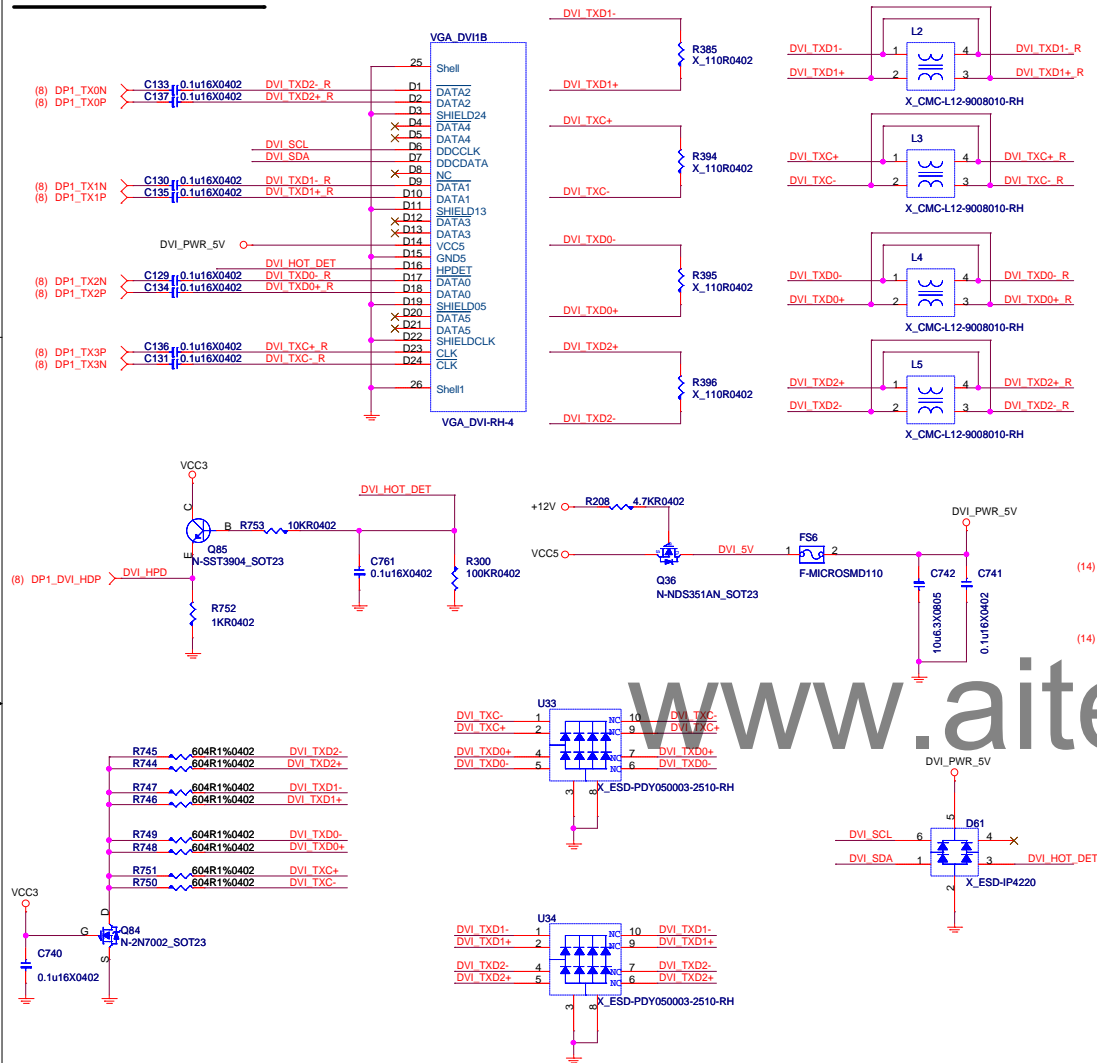
NEAR USB REAR CONNECTOR



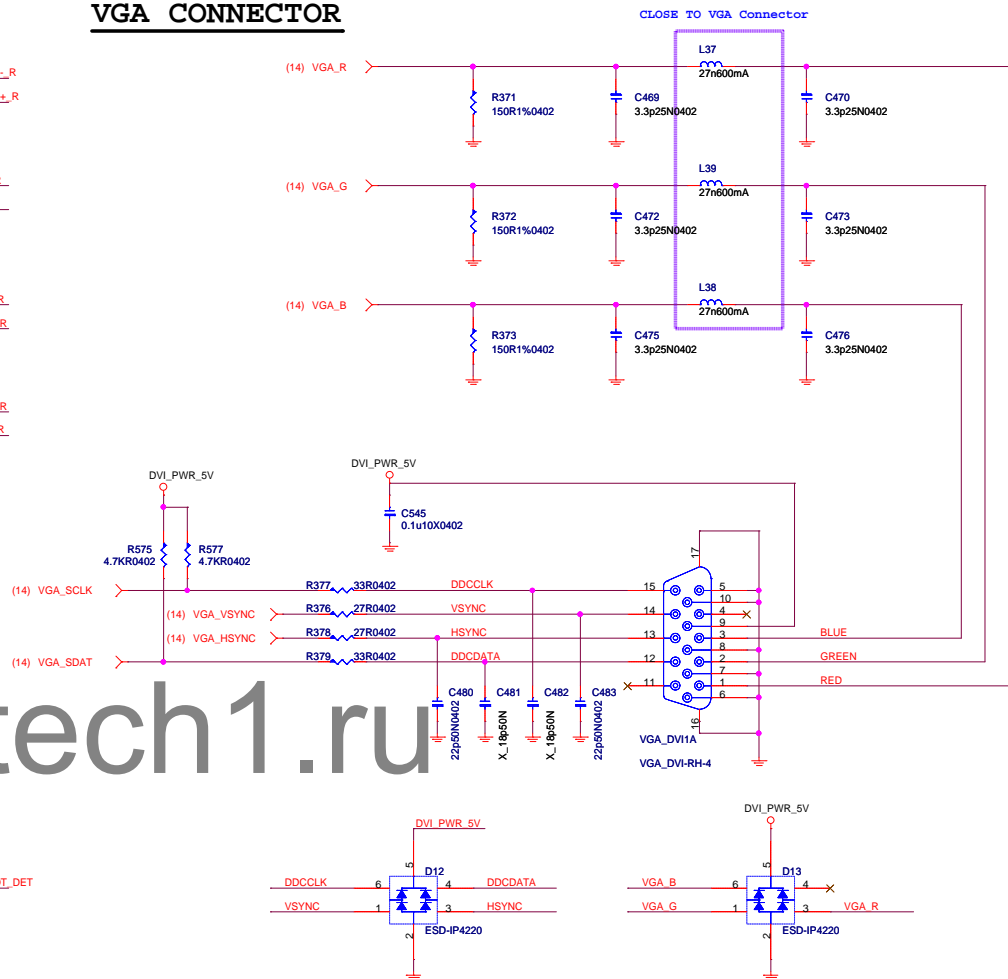
NEAR USB Front CONNECTOR



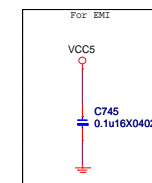
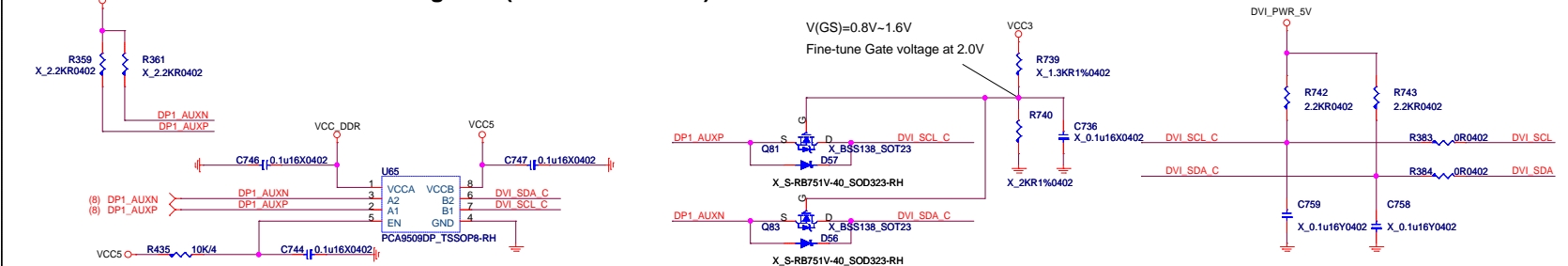
DVI CONNECTOR



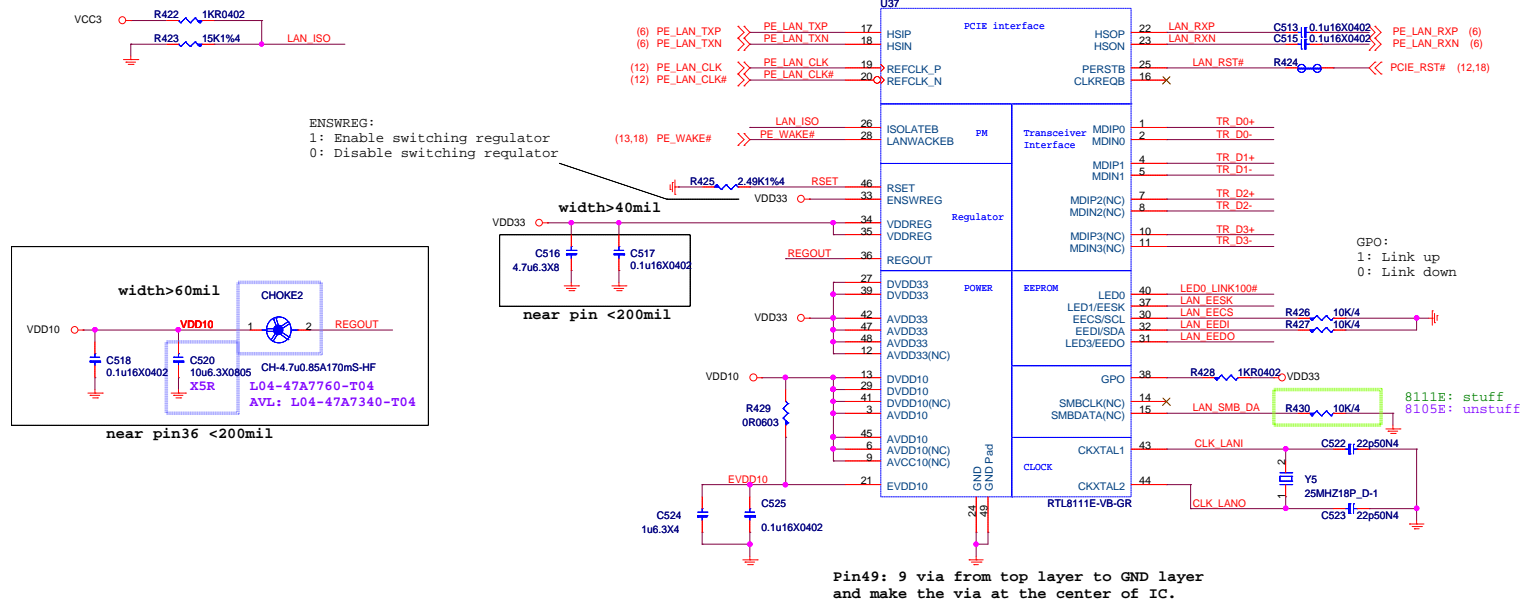
VGA CONNECTOR



LEVEL SHIFT using MOS(Fairchild BSS138)

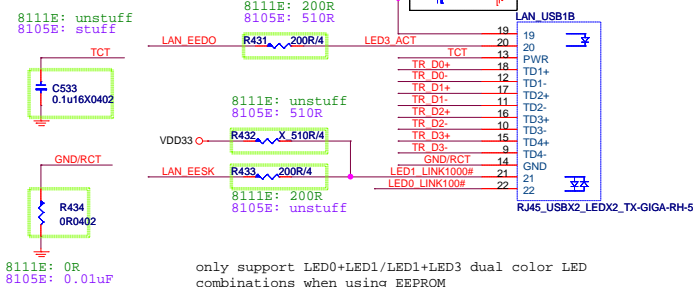
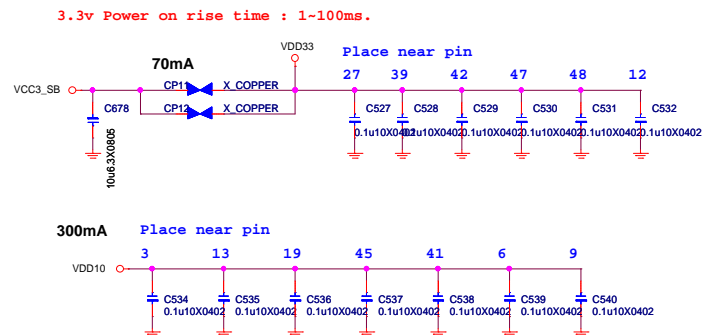


RTL8111E/8105E



Pin49: 9 via from top layer to GND layer
and make the via at the center of IC.

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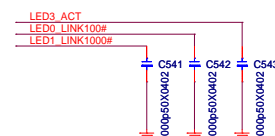
only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM

8105E POWER Consumption

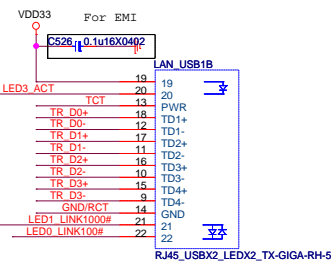
	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

8111E POWER Consumption

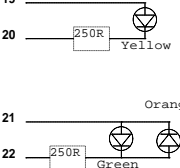
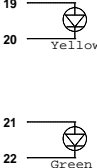
	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

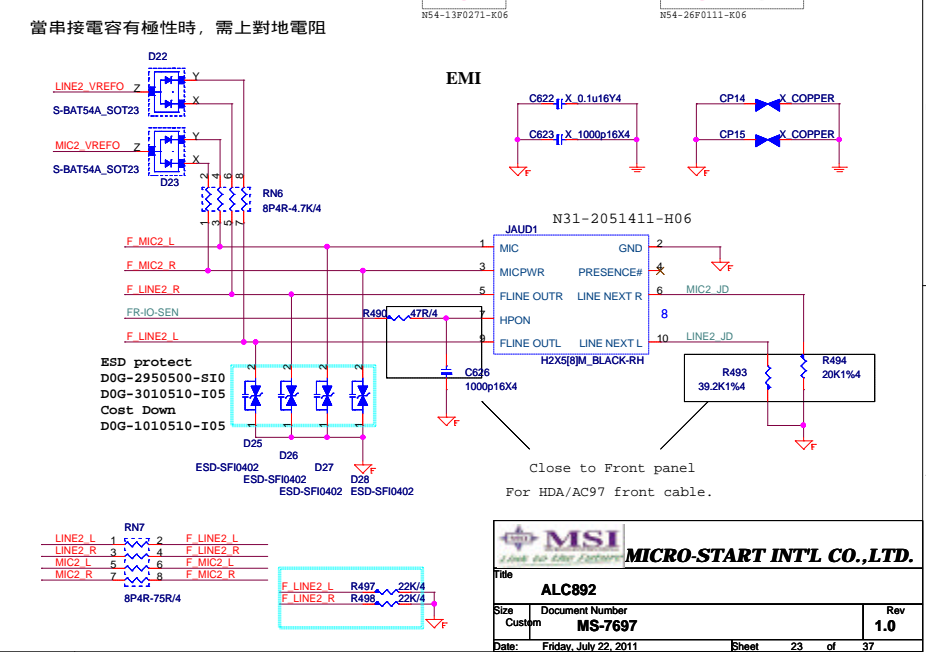
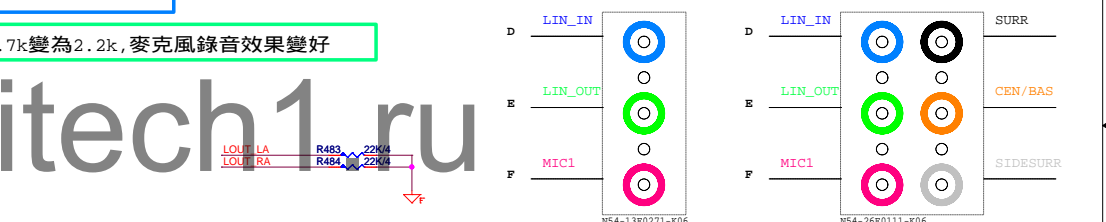
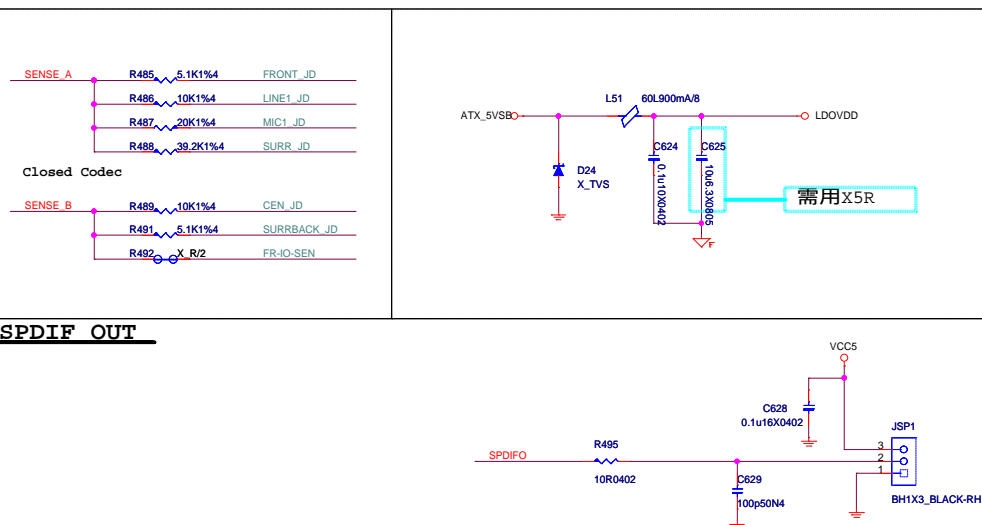
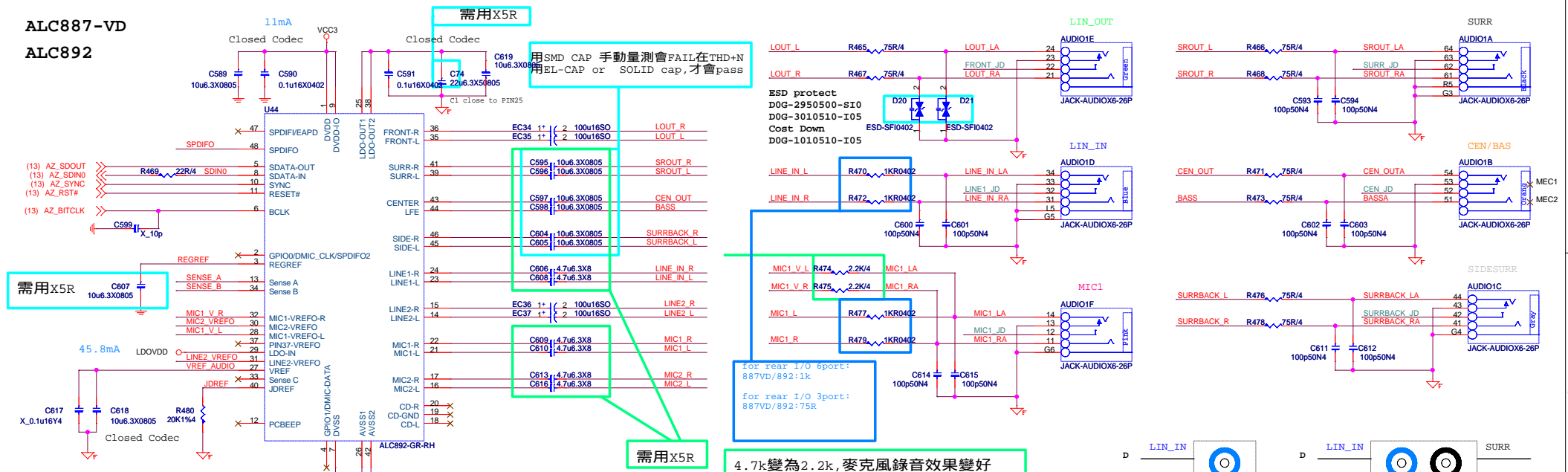


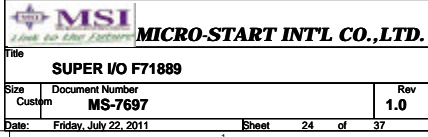
LAN Connector



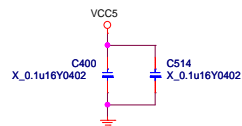
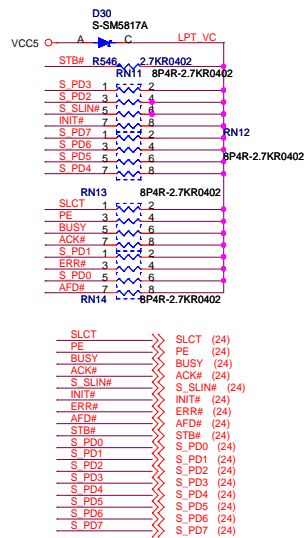
2pF	1pF
D0G-0200529-A68	D0G-0422003-P03
D0G-0303309-C12	D0G-0422003-N47

Giga-Lan		10/100-Lan	
N58-22F0731		N58-22F0771	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		
			

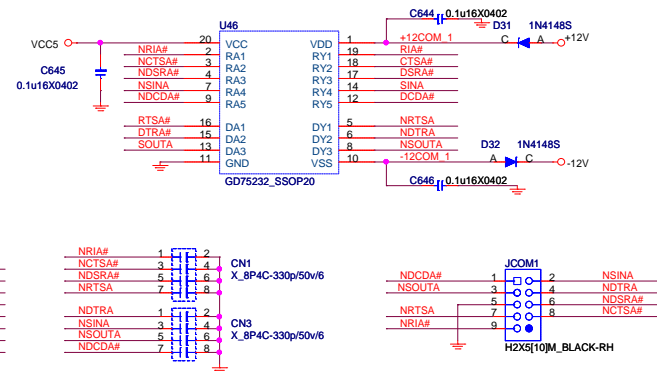
ALC887-VD
ALC892



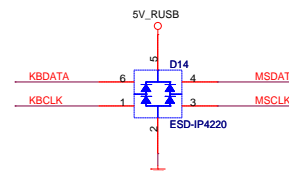
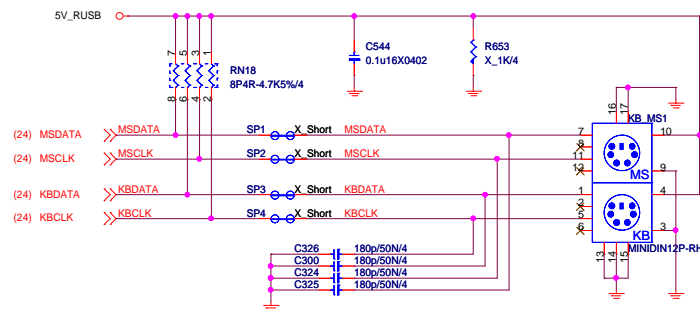
PARALLAL PORT

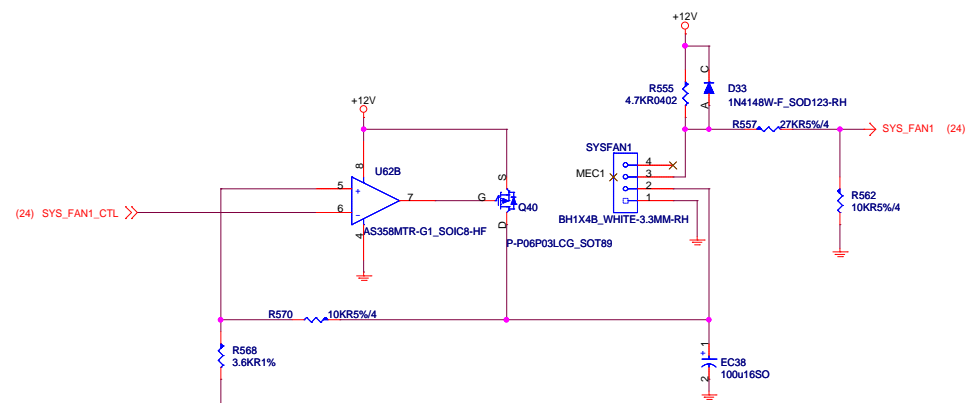


SERIAL PORT 1

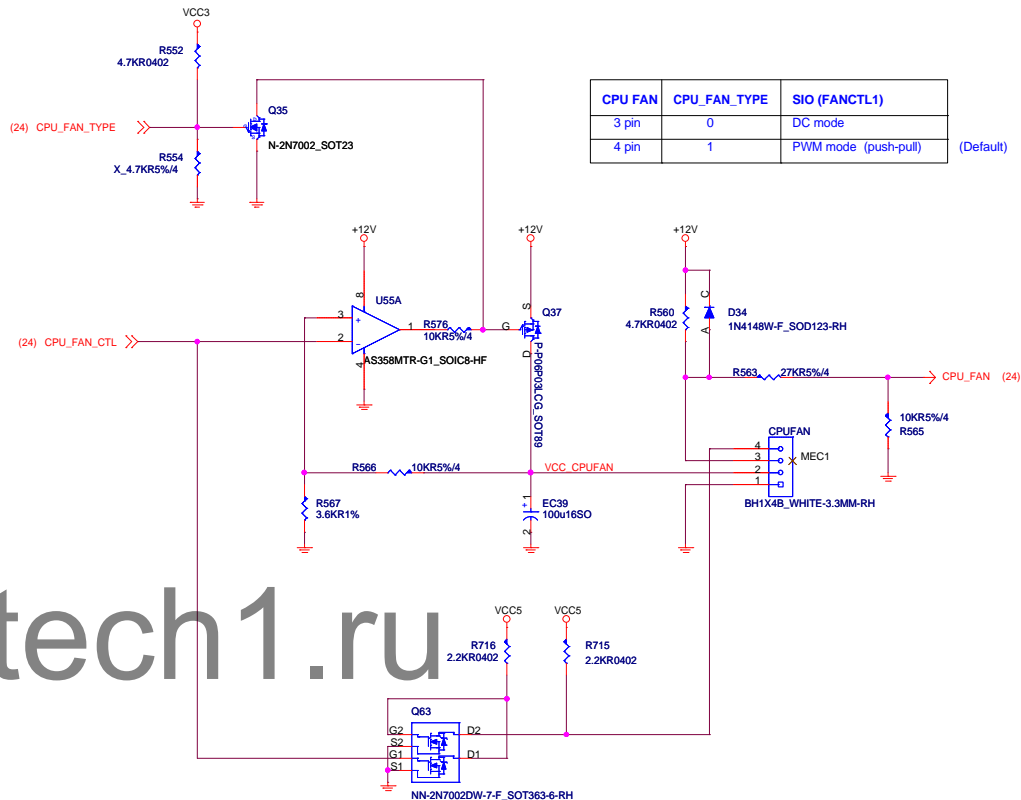


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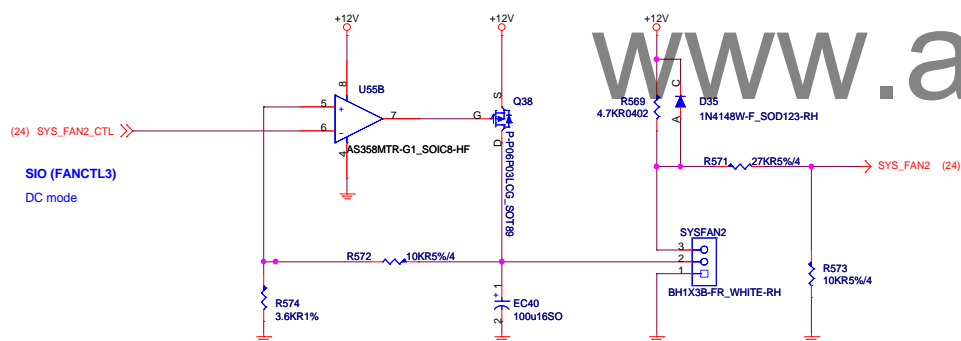




SIO (FANCTL2)
PWM mode



CPU FAN	CPU_FAN_TYPE	SIO (FANCTL1)
3 pin	0	DC mode
4 pin	1	PWM mode (push-pull) (Default)



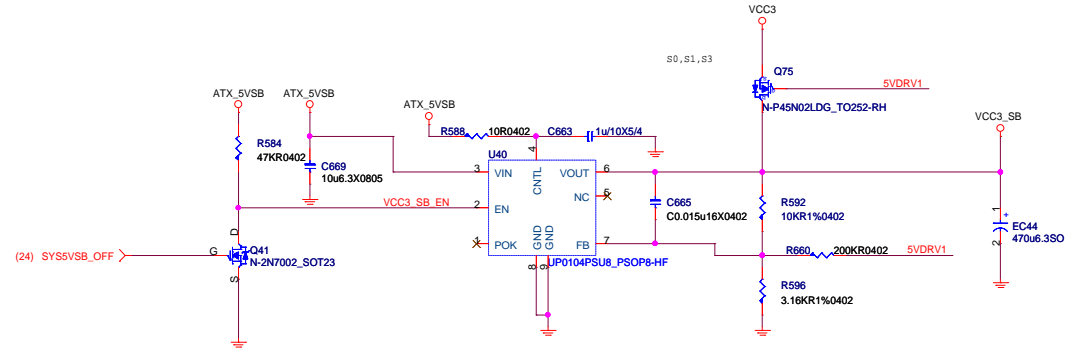
SIO (FANCTL3)
DC mode

VCC5_SB Power Switch

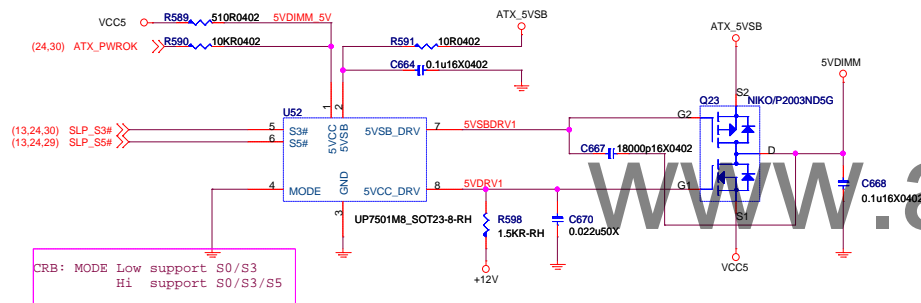
Trace Width 80mils.



VCC3_SB POWER



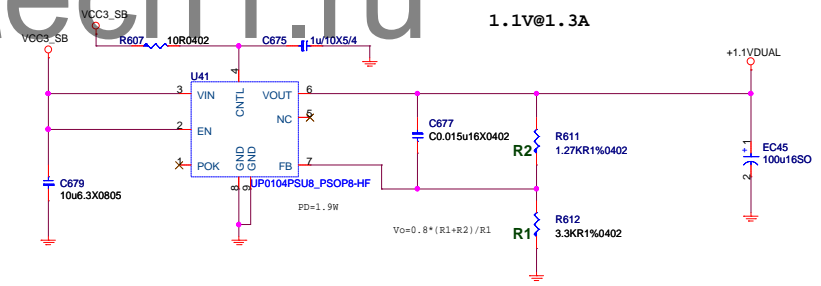
5VDIMM FOR DDR



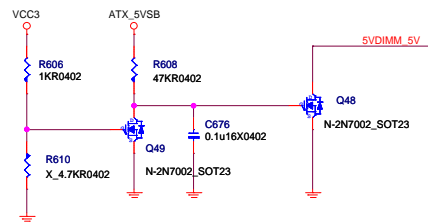
1.1VDUAL POWER

(3.3-1.1) X 1.3 = 2.86W > Po

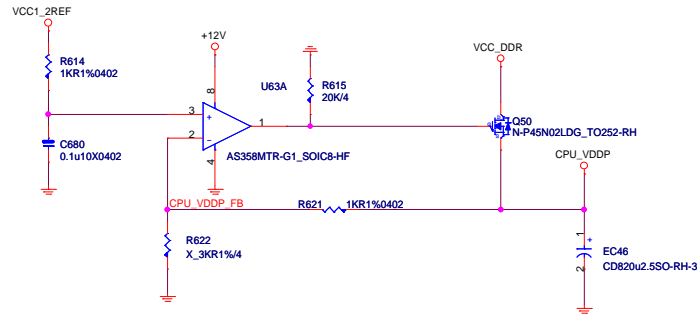
1.1V@1.3A



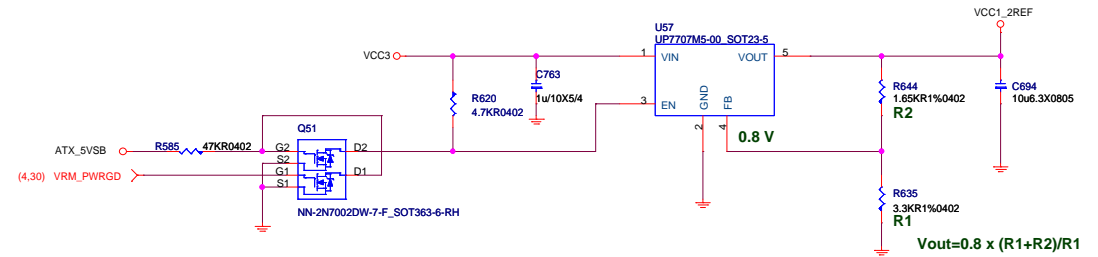
For special PSU sequence



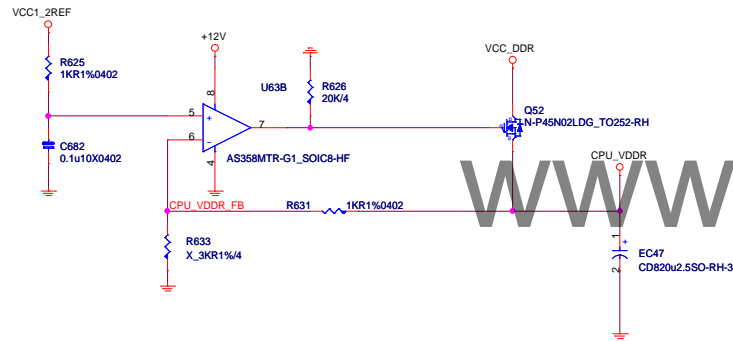
CPU VDDP POWER 1.2 V@3.5A



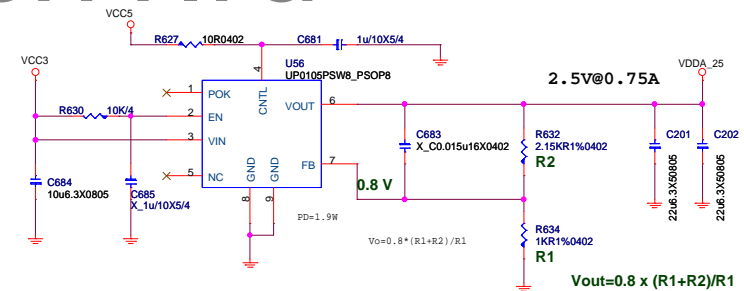
VCC1_2REF



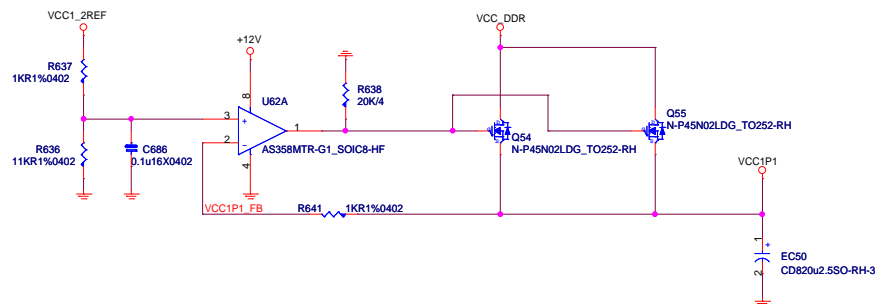
CPU VDDR POWER 1.2 V@4A



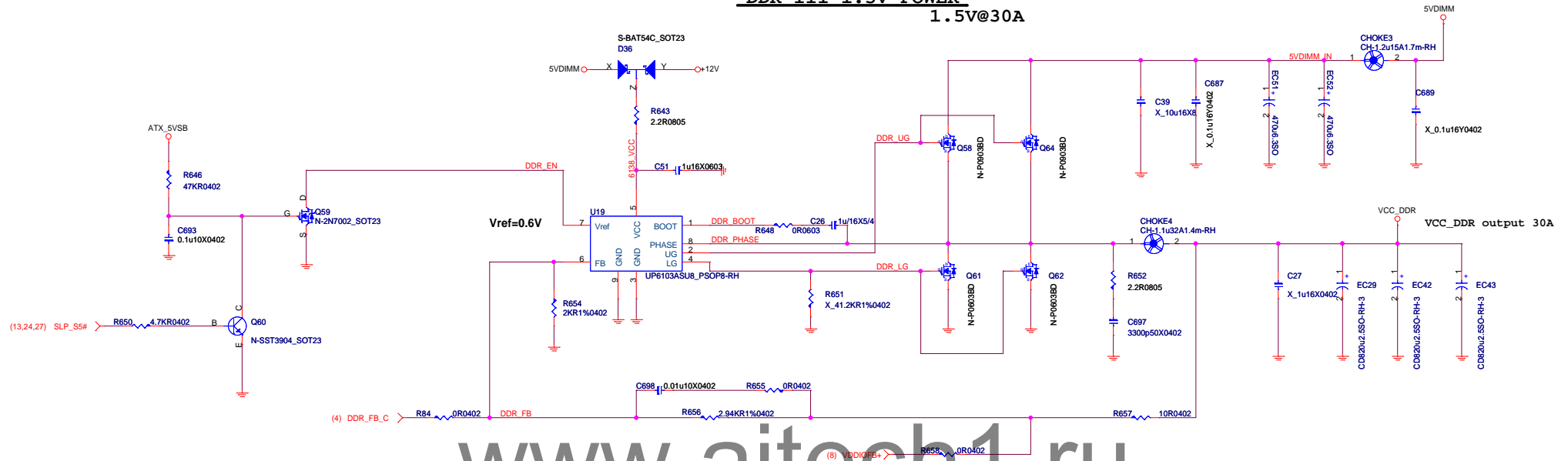
CPU VDDA_25 POWER



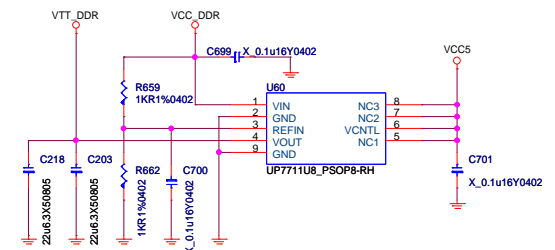
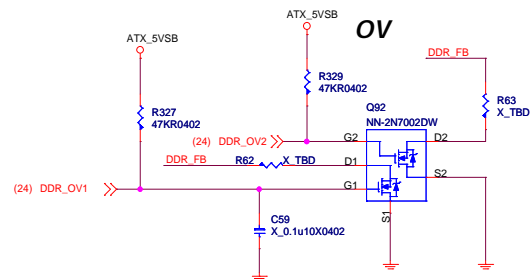
VCC1P1 POWER 1.1V@4.5A+1.3A



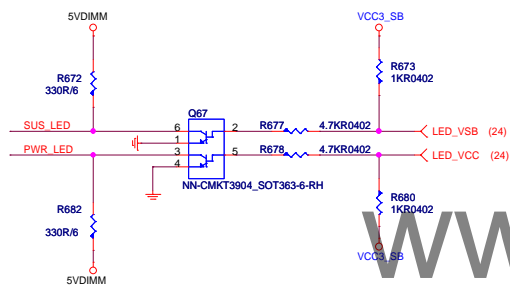
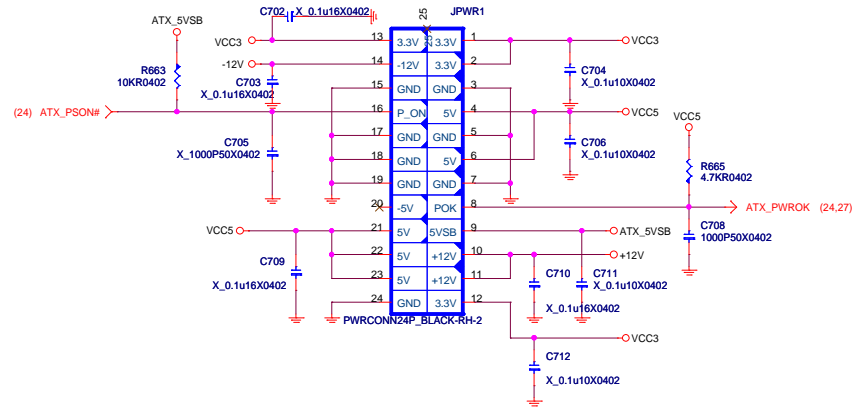
DDR III 1.5V POWER
1.5V@30A



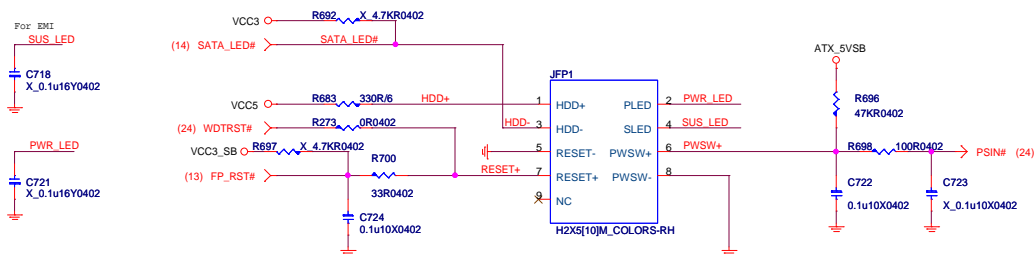
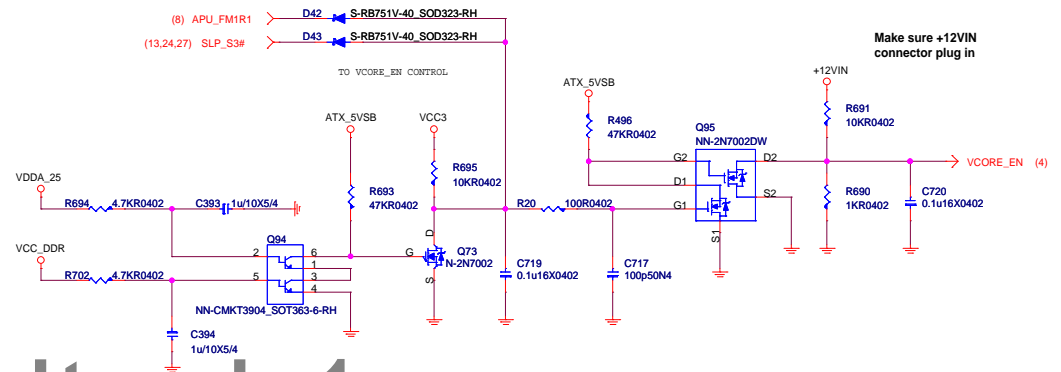
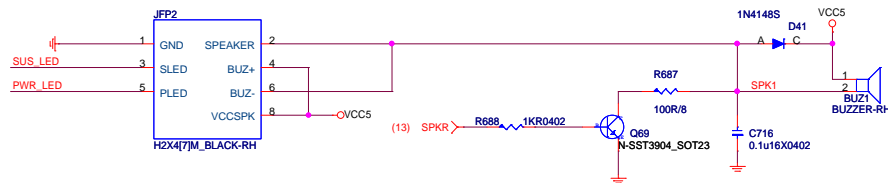
0.75V@2A VTT_DDR POWER



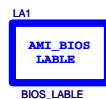
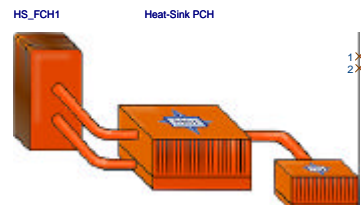
ATX CONNECTOR



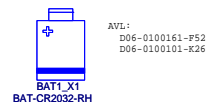
BUZZER



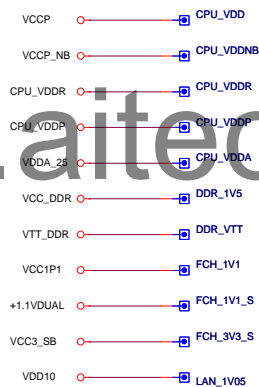
HEAT SINK



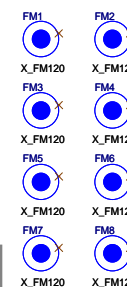
MANUAL PART



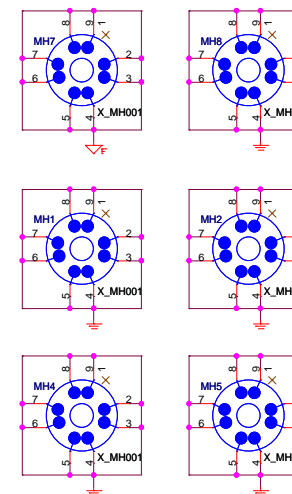
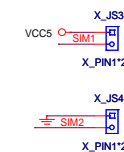
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PK0-0769710-E48, 競華, 23, 寶安恩斯通廠 (MSIS)
PK0-0769710-E48, 競華, 77, 寶安恩斯通廠 (MSIS)




Optics Orientation Holes



Simulation



		MICRO-START INT'L CO.,LTD.	
Title Auto BOM Mnaual			
Size	Custom	Document Number	Rev
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Circuits


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